REMARKS

In response to the Official Action mailed October 23, 2002, Applicants amend their application and request reconsideration. No claims are added, cancelled, or amended.

The Examiner pointed out that reference numbers 12 and 42 appearing in certain figures are not described in the patent application. In response, a proposed drawing correction is submitted, eliminating those reference numbers from the drawing figures, the same action taken in response to the same rejection in the parent patent application. In addition, a set of formal drawings, incorporating this change and other changes is also submitted.

As requested, a substitute title is supplied.

Although claims 7 and 8 were stated to be allowable, the claims 6, 9, and 10 were rejected as anticipated by Kosaki et al. (U.S. Patent 5,872,396, hereinafter Kosaki). This rejection is respectfully traversed.

In rejecting claims 6, 9, and 10, the Examiner recited the language of claim 6 at page 4 of the Official Action. Citing that language, the Examiner asserted, without citing any reference numbers from the figures of Kosaki, that "the second metal layer has a top portion located below the first main surface." This limitation does not appear in Kosaki.

Referring to the embodiment of Figure 1K of the present patent application, it is apparent that the second metal layer 4 has a topmost portion located below the first main surface of the semiconductor substrate 1. What that description means, as clearly explained in the present patent application, is that the second metal layer is absent from the first main surface of the semiconductor substrate and, in fact, does not even reach that first main surface. That arrangement is clearly described in claim 6 by stating that the second metal layer is "below" the first main surface. Because it is apparent there has been a misinterpretation of the claim language, the language is clarified, without substantive change, by explaining that "below" means separated from, i.e., spaced from, the first main surface of the semiconductor substrate as illustrated in the embodiments of the invention shown in Figures 1K, 2B, and 4 of the patent application. This arrangement is in substantial contrast with the prior art described in the patent application, for example the structure shown in Figure 5L which resembles, in pertinent part, the structure shown in Figure 2 of Kosaki. In that prior art structure, the layer 34 is flush with the first main surface of the semiconductor substrate.

As described in the patent application and summarized in the paragraph appearing at page 19 beginning in line 9, an important advantage is achieved in the invention by ensuring that the topmost layer of the flange does not reach the first main surface of the semiconductor substrate. Because of that arrangement, when a bonding wire is bonded to the first main surface of the semiconductor substrate, there is no likelihood of a short circuit to the flange because the

uppermost metal layer of the flange is depressed below the plane of the first main surface of the semiconductor substrate.

Since Kosaki does not disclose the structure of claim 6, that patent cannot anticipate claim 6 or any other pending claim of this patent application. Accordingly, reconsideration and withdrawal of the rejection are earnestly solicited.

Respectfully submitted,

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